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Description

This invention relates to a matrix-addressed display device that displays for example a TV picture, more particularly to the construction of a sampling frequency generator in serial-parallel conversion by sampling the input picture signal.

Recent years have witnessed rapid advances in the technology of TV picture display terminals employing matrix-addressed display elements using liquid crystals, and some of these advances have reached the stage of being utilized in practice. In such matrix-addressed display devices, the video signal has to be supplied to a large number of signal lines and sampling used to perform serial-parallel conversion on the TV signal etc., which is in the form of a dot-sequential signal.

"Serial-parallel conversion" means that serial data, i.e. data that is time-serially transmitted on a single transmission line, is converted to parallel data that is simultaneously transmitted on a plurality of transmission lines. Such serial-parallel conversion is utilized in a matrix-addressed display device that is driven by one-line-at-a-time addressing.

A typical matrix-addressed liquid crystal display device has a rectangular display panel consisting of thin film transistors (TFT) arranged in a matrix constituted by the points of intersection of respective signal lines X1, ..., Xm and address lines Y1, ..., Yn, which are provided in the horizontal direction (X axis direction or main addressing direction) and vertical direction (Y axis direction or ancillary addressing direction). To display a picture, the temporarily stored serial picture signal is supplied in parallel to all of the signal lines X1, ..., Xm, simultaneously, and then selected and displayed by the address lines Y1, ..., Yn. Each scan of the address lines gives one picture frame.

To operate this matrix display, a picture signal source, frame inverting amplifier, synchronizing signal separator, control circuit, Y driver and X driver are arranged around the periphery of the display panel. The X driver is provided with a sampling pulse generator and sample and hold circuit. The picture elements within the liquid crystal display panel are constituted by a TFT, a signal storage capacitor, a liquid crystal cell and a counter electrode common to all the picture elements.

Fig. 6 is a waveform diagram given in explanation of the operation of such a display device, a and b are respectively the vertical synchronizing signal and horizontal synchronizing signal obtained at the output of the synchronizing signal separator, c is the vertical scanning start signal. This is generated under the control of the abovementioned synchronizing signals. Horizontal synchronizing signal b and vertical scanning start signal c are fed to the Y driver to address, one line at a time, the address lines Y1, ..., Yn of the liquid crystal display panel. Also d is the picture signal. This is supplied from the picture signal source through the frame inverting amplifier to the sample and hold circuit. The drawing shows the period of a single horizontal scan. e1 and f are respectively the sampling frequency signal and horizontal scanning start signal. These signals are generated under the control of the horizontal synchronizing signal b. It should be noted that, in the Figure, the length of the time axis of the other signals shown below signal d is the same as in the case of signal d itself.

Of these, the sampling frequency signal e1 and the horizontal scanning signal f are supplied to the sampling pulse generator, which is constituted by a shift register, and generates sampling pulses S1, ..., Sm. These sampling pulses S1, ..., Sm are supplied to the sample and hold circuit, which converts the picture signal d into a parallel picture signal by a sequential sample-and-hold operation performed with the period of the horizontal scanning. When this conversion is completed, the parallel picture signal is simultaneously delivered, under the control of output enable pulse g from the control circuit, from the sample and hold circuit to the signal lines X1, ..., Xm of the liquid crystal panel. This causes the picture signal voltage to be written from the signal lines X1, ..., Xm into the signal storage capacitors, through those TFT which are in an on-state as a result of one or other of the address lines Y1, ..., Yn having been put into the selected state by the vertical scanning pulse from the Y driver. The picture is displayed by excitation of the liquid crystal cells by the picture signal voltage, which is held for the frame scanning period.

However, in a typical prior art display device, the sampling frequency generator is provided in the control circuit, for example as shown in U.S. 4,393,405. Fig. 7 shows the construction of a frequency synthesizer in which a PLL (Phase-Locked Loop) is utilized as this sampling frequency generator. As shown in Fig. 7, this sampling frequency generator is composed of a voltage controlled oscillator 10, a counter 11, a phase comparator 12, a low pass filter 13, a reference frequency input terminal 14 and an oscillating frequency output terminal 15. By setting the count of counter 11 to a desired value, for example K, this enables a frequency of K times the horizontal synchronizing frequency, as shown in e1 of Fig. 6, to be obtained at oscillating frequency output terminal 15 when the horizontal synchronizing signal shown at b of Fig. 6 is supplied to reference frequency input terminal 14.

However, with a matrix-addressed display device as described above, if the sampling frequency generator is constructed of a PLL, fine picture display is difficult to obtain, due to disturbance of the sampling timing resulting from frequency or phase instability of the oscillating output pulse. Furthermore, power is consumed unnecessarily by the fact that the oscillating pulse from the sampling frequency pulse generator is output continuously, even in periods wherein a sampling pulse is not required, such

as the period where the output enable pulse g of Fig. 6 is high level.

This invention provides a matrix-addressed display device capable of displaying clear pictures with low power consumption.

Accordingly the present invention provides a matrix-addressed display device comprising a sampling frequency signal generator, a sampling pulse generator generating sampling pulses in response to the output of the sampling frequency signal generator, means for sampling a serially input video signal with the sampling pulses, means for holding the sampled signal and converting it from serial to parallel, and picture display means utilizing the serial-parallel converted signal, characterized in that the sampling frequency generator includes a gated oscillator employing a logic gate which performs free-running oscillation and means for suspending operation of the gated oscillator in periods im which the serial-parallel conversion is not required.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings in which:

Fig. 1 is a block diagram showing an embodiment of this invention.

Fig. 2 is a circuit diagram showing major parts of Fig. 1.

Fig. 3 is a waveform diagram given in explanation of Fig. 2.

Fig. 4 is a circuit diagram of major parts of another embodiment of this invention.

Fig. 5 is a waveform diagram given in explanation of Fig. 4.

Fig. 6 is a waveform diagram given in explanation of the operation of the matrix-addressed display device.

Fig. 7 is a block diagram showing an example of the sampling frequency generator of a conventional device.

Fig. 1 shows a matrix-addressed display device constituting an embodiment of this invention. The basic construction of this matrix-addressed display device involves producing a display such as a television picture using a thin film transistor TFT array type liquid crystal display panel. As shown in the Figure, signal lines X1, ..., Xm and address lines Y1, ..., Yn are arranged in an intersecting manmer within the liquid crystal display panel 1, while a picture signal source 2, a frame inverting amplifier 3, a synchronizing signal separator 4, a control circuit 5, a Y driver 6, and an X driver 7 are provided around the periphery of the panel. X driver 7 consists of a sampling pulse generator 7_1 and a sample and hold circuit 7_2. Pixels 8 in the liquid crystal display panel 1 are composed of respective TFT 8_1, signal storage capacitor 8_2, liquid crystal cell 8_3 and counter electrode 8_4.

Specifically, the output signal from picture signal source 2 is applied to frame inverting amplifier 3 and synchronizing signal separator 4. The subsequent waveforms of each signal coincide with the corresponding symbols a to g of Fig. 6. Synchronizing signal separator 4 separates vertical synchronizing signal a and horizontal synchronizing signal b from the aforementioned signal and supplies them to control circuit 5. Frame inverting amplifier 3 generates picture signal d, inverted in polarity with every frame, in synchronism with the signal from the control circuit, and supplies it to sample and hold circuit 7_2.

Control circuit 5 receives vertical synchronizing signal a and horizontal synchronizing signal b and supplies horizontal synchronizing signal b and vertical scanning start signal c, which is synthesized from the synchronizing signals a and b, to Y driver 6. Furthermore, control circuit 5 generates sampling frequency signal e2 and horizontal scanning start signal f based on horizontal synchronizing signal b, and delivers them as input to sampling pulse generator 7_1. It also delivers output enable pulse g from this circuit 5 to sample and hold circuit 7_2.

Sampling pulse generator 7_1 receives signals e2 and f and generates sampling pulses S1, ..., Sm. These sampling pulses S1, ..., Sm are supplied to sample and hold circuit 7_2, which successively samples and holds picture signal d at each horizontal scanning period, to convert it into a parallel picture signal. When this conversion is complete, the parallel picture signal is simultaneously delivered from sample and hold circuit 7_2 to signal lines X1, ..., Xm of liquid crystal display panel 1, under the control of output enable pulse g from control circuit 5. At this point, the video signal voltage is written into signal storage capacitor 8_2 from signal lines X1,..., Xm through the TFT 8_1 which has been put into a conductive state by one or other of the address lines Y1, ..., Yn being put in a selected state by the vertical scanning pulse from Y driver 6. This video signal voltage is held throughout the frame scanning period so that picture display is effected by excitation of the liquid crystal cells 8_3 by this held voltage.

In this embodiment, the aforementioned sampling frequency generator has special features.

This sampling frequency generator is described in more detail with reference to Fig. 2. This sampling frequency generator consists of: gated oscillator 20, horizontal counter 21, inverter 22, D type flip-flop 23, monostable multivibrator 24, and horizontal synchronizing signal input terminal 25. Gated oscillator 20 is constituted by: 2-input NAND gate 20_1, inverter 20_2, buffer 20_3, control input terminal 20_4, input terminal 20_5 for constituting the oscillating circuit, output terminals 20_6, 20_7, resistor 20_8 for determining the frequency of oscillation, capacitor 20_9 and sampling frequency output terminal 20_{10}.

Fig. 3 is a waveform diagram given in explanation of the operation of the embodiment shown in Fig. 2. First of all, when horizontal synchronizing pulse b, which is either contained in the input video signal or separately supplied is supplied to the horizontal synchronizing input terminal 25, at the output $\overline{Q}$ of the monostable multivibrator; pulse h1 is obtained, of width determined by the

resistor 24_1 and capacitor 24_2. On the rising edge of for example pulse h1 of timing related to the horizontal synchronizing signal, output Q of flip-flop 23 changes from low level to high level as shown by waveform h2, starting the oscillation of gated oscillator 20 using a logic gate, and releasing the reset of horizontal counter 21. Also oscillating output pulse j obtained at output terminal 20_{10} of gated oscillator 20 is counted by being input to horizontal counter 21. The output from output terminal Qm of horizontal counter 21 changes from low level to high level when a number of oscillating pulses j is output, which number is related to the number of pixels in the horizontal direction, being for example equal to or a little greater than the number of pixels in the horizontal direction of the display panel. When the output from output terminal Qm goes to high level, flip-flop 23 is reset, making the output from output terminal Q go to low level. This stops the pulse oscillations of the gated oscillator 20, resets the horizontal counter 21, and returns the output from output terminal Qm to low level. Consequently, the output from output terminal Qm varies in accordance with the waveform k. When horizontal synchronizing pulse b again arrives at the input terminal 25, the sequence of events described above is repeated.

In this embodiment, for the sampling frequency signal, the frequency of oscillation of the gated oscillator 20 can be selected using the resistor 20_8 and capacitor 20_9, and the time-point at which oscillations start can be controlled by the resistor 24_1 and the capacitor 24_2 of the monostable multivibrator 24. Furthermore, a sampling pulse for the input video signal as shown in Fig. 3 g1, ..., gm can be obtained if a horizontal scanning start pulse l is formed as shown in Fig. 3 and supplied to sampling pulse generator 7_1 of Fig. 1 together with pulse j.

In this embodiment, the generation of the sampling frequency signal is by free-running oscillation, so there is no fluctuation of frequency or phase. Also, since the sampling frequency generator is constituted by a gated oscillator, starting and stopping of oscillation can be controlled so that the sampling frequency signal is generated only in the period of display of the video signal during horizontal scanning. This makes it possible to save power by reducing the number of switching operations.

Fig. 4 shows a further embodiment of this invention. Parts which are the same as in the embodiment of Fig. 1 and Fig. 2 are given the same reference numerals. Further to the embodiment of Fig. 2, this embodiment is equipped with vertical synchronizing signal input terminal 30, monostable multivibrator 31, D type flip-flops 32 and 33, vertical counter 34 and 2-input OR gate 35.

Fig. 5 is a waveform diagram showing the operation of the embodiment shown in Fig. 4. First of all, when vertical synchronizing pulse a, which is the vertical synchronizing signal either contained in the input video signal or separately input, is supplied to vertical synchronizing signal input terminal 30, pulse m of width determined by resistor 31_1 and capacitor 31_2 is obtained at output $\overline{Q}$ of monostable multivibrator 31. This pulse m is input to the flip-flop 32, and clock-synchronized with output pulse n of monostable multivibrator 24, which has the period of the horizontal scan, to obtain pulse p at output Q of flip-flop 32. On the leading edge of pulse p, the output $\overline{Q}$ of flip-flop 33 changes from high level to low level as shown by the waveform q, releasing the reset of flip-flop 23 and opening the circuit from output Qm of horizontal counter 21 to reset terminal R of flip-flop 23. This starts the operation of the portion which is the same as in the embodiment of Fig. 2. At the same time as this, the reset of vertical counter 34 is released, so that pulses n which are being input are counted by vertical counter 34. At the time-point when a number of these pulses n which is related to the number of pixels in the vertical direction of the display panel and is for example equal to or slightly greater than this number of pixels has been output, the output from output terminal Qn of vertical counter 34 changes from low level to high level. When the output from output terminal Qn becomes high-level, flip-flop 33 is reset, with the result that the output from output terminal $\overline{Q}$ becomes high-level. Flip-flop 23 is then reset by means of 2-input OR gate 35, and vertical counter 34 is also reset, causing the output from output terminal Qn to return to low level. The output from output terminal Qn therefore varies as waveform r, and the output from output terminal Q of flip-flop 23 varies as waveform s. Thus operation of the portion that is the same as in the Fig. 2 embodiment is stopped at the time-point when vertical counter 34 has counted the prescribed number of output pulses n. The sequence of operations described above is repeated when vertical synchronizing pulse a is again supplied.

In addition to providing the same effect as the preceding embodiment, this embodiment enables the portion corresponding to the preceding embodiment to be started and stopped in response to whether the output from output terminal $\overline{Q}$ of flip-flop 33 is high or low. That is, a further power saving can be obtained thanks to the fact that oscillation of gated oscillator 20 and counting by horizontal counter 21 do not take place whilst output terminal $\overline{Q}$ of flip-flop 33 is high-level.

In the above two embodiments, the oscillating circuit of gated oscillator 20 is constructed using resistor 20_8 and capacitor 20_9. However, the invention is not restricted to this, and the oscillating circuit may be constructed using for example an inductor and a capacitor, or if the sampling frequency or dot clock is input from outside together with the video signal, resistor 20_8 of gated oscillator 20 can be dispensed with, and input terminal 20_5 utilized as the sampling frequency input terminal.

As described above, since the matrix-addressed display device of this invention employs as the sampling frequency generator a gated oscillator

controlled by a logic gate, a sampling frequency signal with little fluctuation of frequency of phase can be generated and a clear picture obtained, and a considerable saving in power can be obtained, thanks to the fact that its operation is stopped in periods when generation of a sampling frequency signal is not required. This saving is particularly great if a CMOS circuit construction is used.

Claims

1. A matrix-addressed display device comprising a sampling frequency signal generator (5), a sampling pulse generator (71) generating sampling pulses (s1, ..., sm) in response to the output of the sampling frequency signal generator, means (72) for sampling a serially input video signal (d) with the sampling pulses (s1, ..., sm), means for holding the sampled signal and converting it from serial to parallel, and picture display means (1) utilizing the serial-parallel converted signal, characterized in that the sampling frequency generator includes a gated oscillator (20) employing a logic gate (201) which performs free-running oscillation and by means for suspending operation of the gated oscillator in periods in which the serial-parallel conversion is not required.

2. A matrix-addressed display device according to claim 1 wherein the means for suspending operation of the gated oscillator includes a horizontal counter (21) which counts the pulse output from the sampling frequency signal generator up to a predetermined number of horizontal pixels relative to a horizontal synchronization input signal and supplies a control signal to the logic gate of the gated oscillator.

3. A matrix-addressed display device according to claim 2 wherein the means for suspending operation of the gated oscillator further includes a vertical counter (34) counting the input horizontal synchronization signal up to a predetermined number of vertical pixels relative to a vertical synchronization input signal and supplies a control signal to the logic gate of the gated oscillator.

Patentansprüche

1. Matrixadressierte Anzeigeeinrichtung mit einem Tastfrequenz-Signalgenerator (5), einem Abtastimpulsgenerator (71), der in Abhängigkeit von Ausgangssignal des Tastfrequenz-Signalgenerators Abtastimpulse (s1, ..., sm) erzeugt, Mitteln (72) zum Abtasten eines seriellen Videoeingangssignals (d) mit den Abtastimpulsen (s1, ..., sm), Mitteln zum Halten des abgetasteten Signals und dessen Umsetzung von seriell in parallel sowie Bildanzeigemitteln (1), die das seriell-parallell umgesetzte Signal verwenden, dadurch gekennzeichnet, daß der Tastfrequenz-Signalgenerator einen ein Logikgatter (201) verwendenden, getasteten Oszillator (2) enthält, der eine freilaufende Schwingung durchführt, sowie durch Mittel zur Unterbrechung des Betriebs des getasteten Oszillators in Perioden, in denen die seriell-parallele Umsetzung nicht benötigt wird.

2. Matrixadressierte Anzeigeeinrichtung nach Anspruch 1, bei der die Mittel zur Unterbrechung des Betriebs des getasteten Oszillators einen Horizontalzähler (21) enthalten, der die am Ausgang des Tastfrequenzen-Signalgenerators auftretenden Impulse bis zu einer vorbestimmten Anzahl von horizontalen Pixeln bezüglich einem horizontalen Synchronisationseingangssignal zählt und ein Steuersignal an das Logikgatter des getasteten Oszillators liefert.

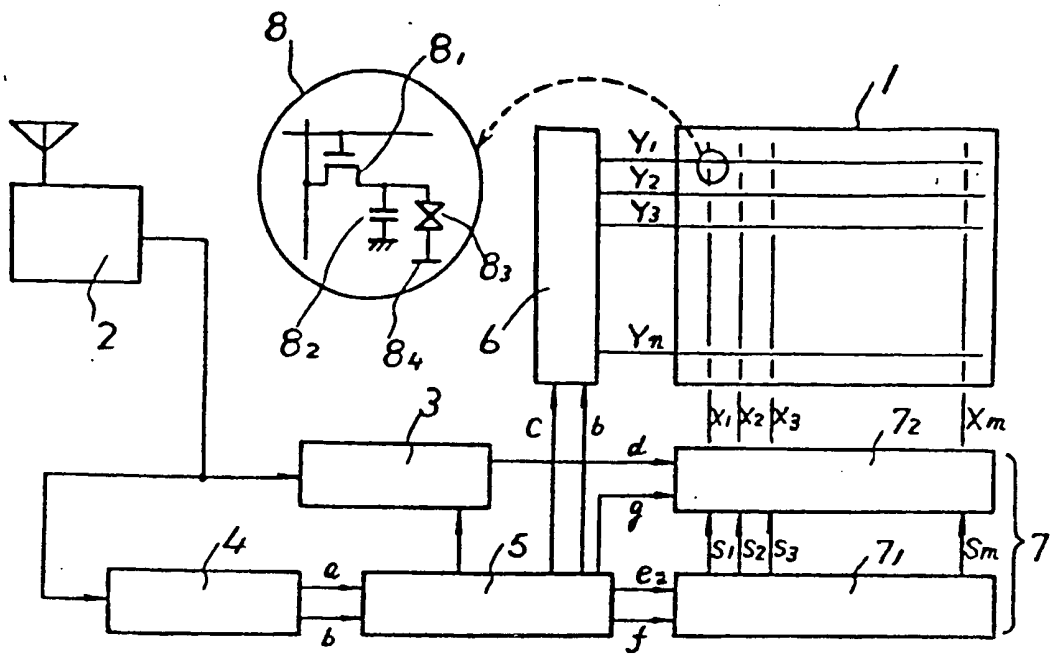
3. Matrixadressierte Anzeigeeinrichtung nach Anspruch 2, bei der die Mittel zur Unterbrechung des getasteten Oszillators ferner einen Vertikalzähler (34) aufweisen, der das horizontale Synchronisationseingangssignal bis zu einer vorbestimmten Anzahl von vertikalen Pixeln bezüglich einem vertikalen Synchronisationseingangssignal zählt und dem Logikgatter des getasteten Oszillators ein Steuersignal zuführt.

Revendications

1. Dispositif d'affichage ou de visualisation à adressage matriciel qui comprend un générateur de signaux de fréquence d'échantillonnage (5), un générateur d'impulsions d'échantillonnage (71) qui produit des impulsions d'échantillonnage (S1, ..., Sm) en réponse aux signaux de sortie du générateur de signaux d'échantillonnage, des moyens (72) pour échantillonner un signal vidéo d'entrée en série avec les impulsions d'échantillonnage, des moyens pour conserver le signal échantillonné et pour le convertir de signal série en signal parallèle, et des moyens d'affichage ou de visualisation d'image (1) utilisant ce signal converti de série en parallèle, est caractérisé en ce que le générateur de fréquence d'échantillonnage comprend un oscillateur à déclenchement ou commandé (20) utilisant une porte logique (201) qui effectue des oscillations libres, et des moyens pour suspendre le fonctionnement de l'oscillateur à porte pendant les périodes pendant lesquelles une conversion série/parallèle n'est pas nécessaire.

2. Dispositif d'affichage, selon la revendication 1, caractérisé en ce que les moyens pour suspendre le fonctionnement de l'oscillateur à déclenchement comprend un compteur horizontal ou de lignes (21) qui totalise les impulsions délivrées par le générateur de signaux de fréquence d'échantillonnage jusqu'à un nombre prédéterminé de pixels horizontaux par rapport à un signal d'entrée de synchronisation horizontale et qui délivre un signal de commande au circuit logique de l'oscillateur à déclenchement.

3. Dispositif d'affichage à adressage matriciel selon la revendication 2, caractérisé en ce que les moyens pour suspendre le fonctionnement de l'oscillateur à déclenchement comprennent aussi un compteur vertical (34) qui totalise les signaux de synchronisation horizontale jusqu'à un nombre prédéterminé de pixels verticaux par rapport à un signal de synchronisation verticale et délivre un signal de commande au circuit logique de l'oscillateur à déclenchement.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Y₁
Y₂
Y₃
Yn
8₃
2
8₂
8₄
6
3
c
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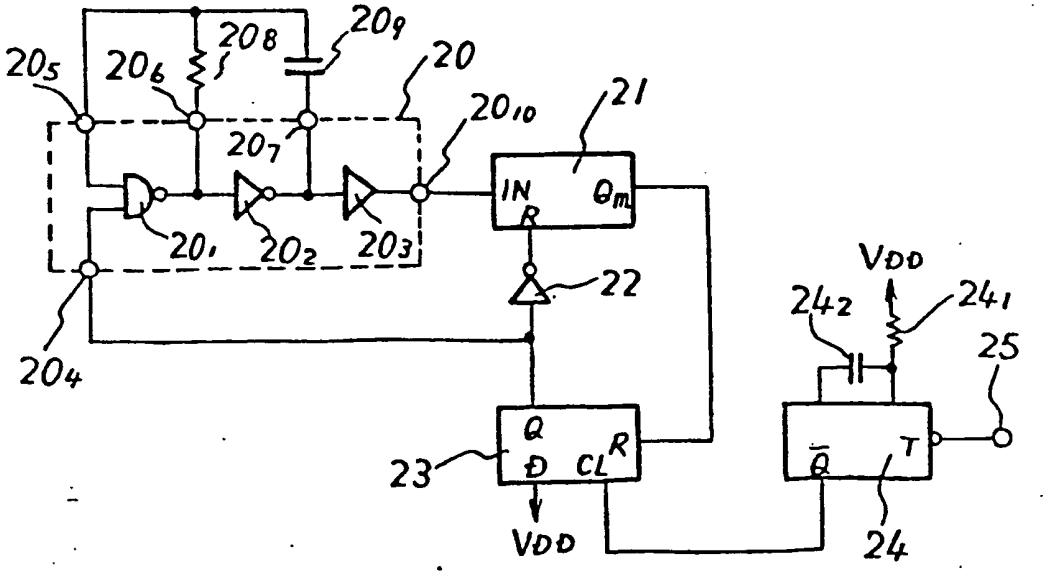
X₁ X₂ X₃
7₂
Xm
g
4
5
a
S₁ S₂ S₃
7₁
Sm
7
e₂
b
f

FIG. 1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R
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20₃
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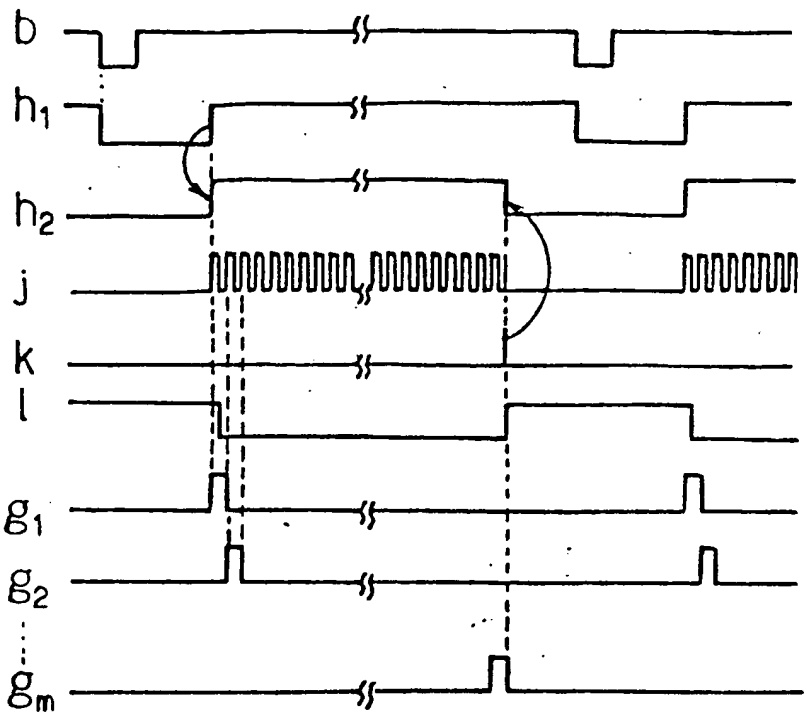
FIG. 2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h2
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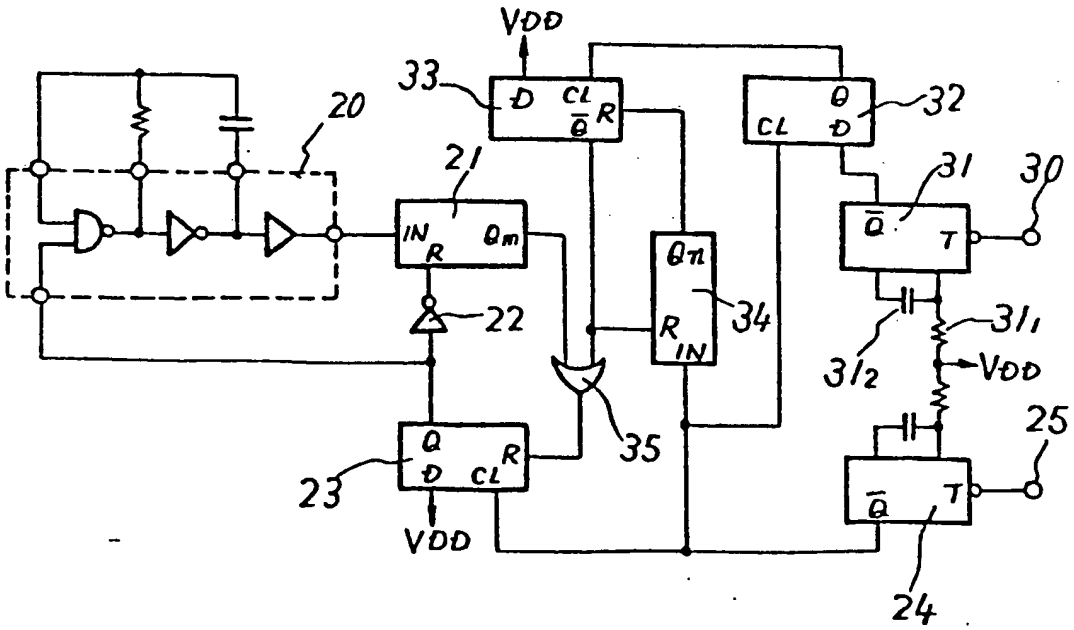
k
l
g1
g2
gm

FIG. 3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D
CL
R
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Qm
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CL
R
23
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T
24

FIG. 4

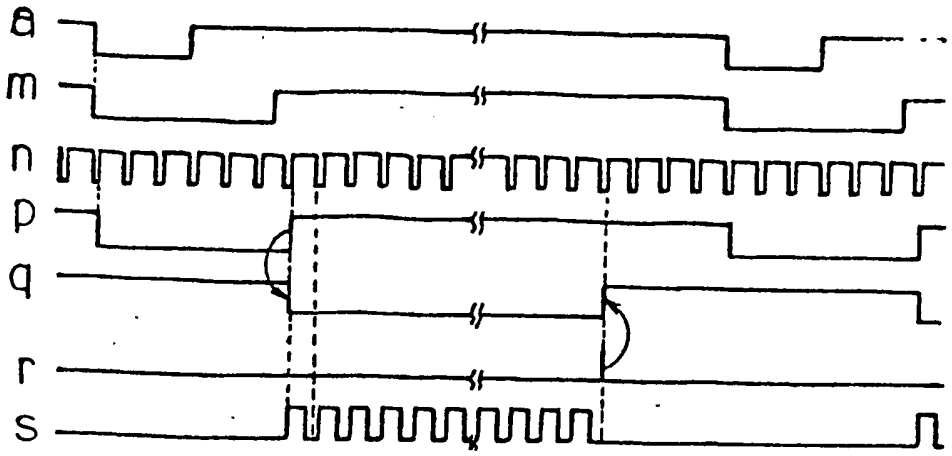

FIG. 5

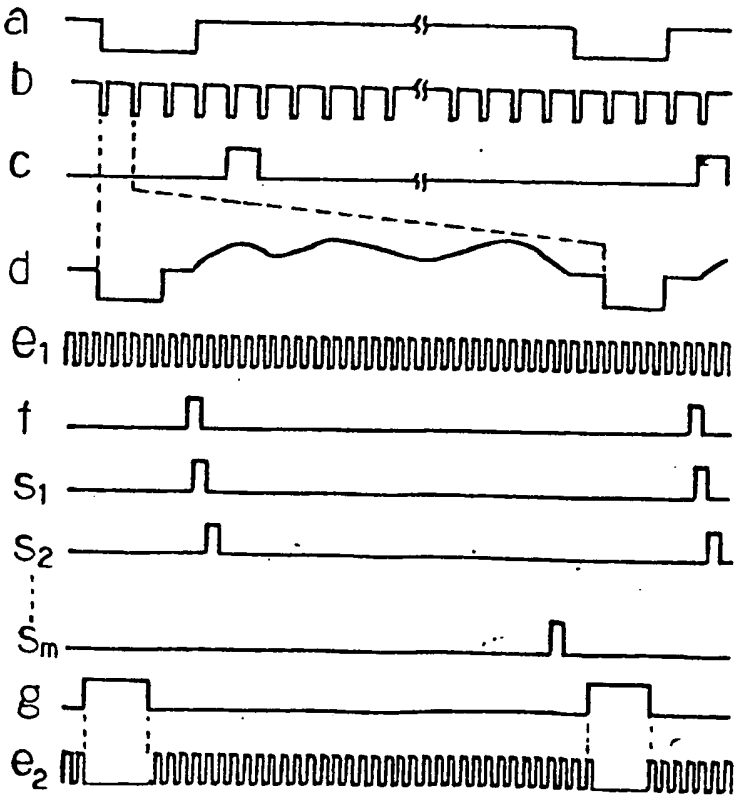

FIG. 6

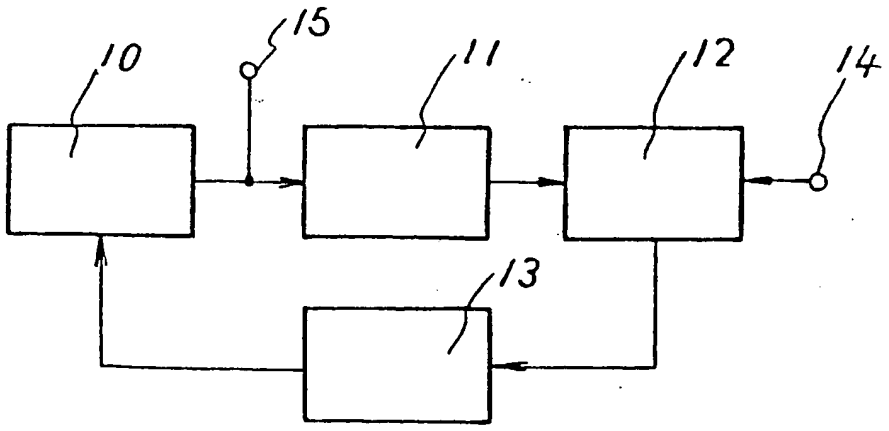

FIG. 7 (PRIOR ART)